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06EC45

Fourth Semester B.E. Degree Examination, June/July 2011
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions selecting atleast TWO questions from each part.***

PART - A

1 a. Mention different types of description in HDL. Explain structural and mixed type of description with example. **(10 Marks)**

b. Explain Verilog data types. **(05 Marks)**

c. Discuss the major differences between VHDL and Verilog. **(05 Marks)**

2 a. Write a VHDL and Verilog code for a 2 × 1 multiplexer in data flow description using signal assignment statement. **(08 Marks)**

b. Write a VHDL code in data flow description for a 2 – bit magnitude comparator with the help of truth table and simplified Boolean expressions. **(12 Marks)**

3 a. Explain CASE statement with syntax. Write a behavioural description of a positive edge-triggered JK flipflop using CASE statement in VHDL and Verilog code. **(10 Marks)**

b. Explain For – loop and while – loop statements in VHDL and Verilog. **(06 Marks)**

c. Write a Verilog code for calculating the factorial of positive integers using while loop. **(04 Marks)**

4 a. What is binding? Discuss binding between a library and component in VHDL. **(06 Marks)**

b. Write the structural description of a D – Latch using VHDL and Verilog code. **(08 Marks)**

c. Briefly explain Generate, Generic and Parameter statements with an example. **(06 Marks)**

PART - B

5 a. Explain the use of procedure in VHDL and task in Verilog with description of an N – bit ripple carry adder. **(10 Marks)**

b. Write a VHDL function to find the larger of two signed numbers. **(06 Marks)**

c. Write a note on Verilog file processing. **(04 Marks)**

6 a. Explain with syntax VHDL package and package body. **(04 Marks)**

b. Write a VHDL code for addition of two 5 × 5 matrices using a package. **(08 Marks)**

c. With a block diagram and function table of SRAM, write a Verilog code for 16 × 8 SRAM. **(08 Marks)**

7 a. Write a mixed Language description of a full adder invoking a VHDL entity from a Verilog module. **(10 Marks)**

b. Write a mixed language description of an AND gate invoking Verilog module from VHDL module. **(06 Marks)**

c. What are the limitations of mixed language description? **(04 Marks)**

8 a. Define synthesis. With flow chart, explain the steps involved in synthesis process. **(08 Marks)**

b. Write VHDL code for signal assignment statement Y = 2 * X + 3. Show the synthesized logic symbol and gate level diagram. Write structural code in Verilog using gate level diagram. **(12 Marks)**

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